GUJARAT TECHNOLOGICAL UNIVERSITY			
C	BE - SEMESTER-III (Old) EXAMINATION – WINTER 2019 Subject Code: 120701		
Su Su	Djeci bioof	Nome: Digital Logia Design	9
Su Tii Inst	Time: 02:30 PM TO 05:00 PM Total Marks:		0
IIIS	1. 2. 3.	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks.	
Q.1	(a)	Convert following Decimal Number to Hex, Binary and octal Number. 1) 157.786 2) 937.125	07
	(b)	Justify the statement: "NAND and NOR gates are universal gates."	07
Q.2	(a) (b)	Expand A+BC'+ABD'+ABCD to minterm and maxterm. Obtain the simplified expressions in SOP for the following Boolean function using K-Map method. And implement it using NAND gate. F(A,B,C,D) = ABC+AB'C+BCD'+A'CD	07 07
	(b)	Simplify the following Boolean function by means of the tabulation method and implement it using NAND gate. $F(A,B,C,D) = \Sigma(0,1,4,7,13,14) + d(5,8,15)$	07
Q.3	(a) (b)	Design a 1:16 demultiplexer using 1:8 demultiplexer. Draw a truth table and logic circuit to realize the following Boolean function using multiplexer. $F(A,B,C,D) = \Sigma (0, 1, 3, 6, 8, 10, 12, 15)$	07 07
Q.3	(a) (b)	With neat logic diagram, explain Universal shift register. Design 4-bit BCD adder using two 4-bit binary parallel adders.	07 07
Q.4	(a)	Draw the characteristics and excitation table of JK flip flop. Design Conversion	07
	(b)	Design 3-bit of any synchronous counter using JK Flip Flop. OR	07
Q.4	(a)	Define following parameters related to logic family and Compare all the logic families based on these parameters :(i) Propagation Delay (ii) Fan-out (iii) Fan-in (iv) Noise margin	07
	(b)	Draw the state diagram of BCD ripple counter, develop it's logic diagram and explain the operation of circuit.	07
Q.5	(a)	Draw the block diagram of a processor unit with control variables and explain its operation	07
	(b)	Discuss the differences between hard wired control & micro program control. State their merits and demerits.	07
0.5	(a)	Explain Register transfer micro operation and arithmetic micro operation	07
~	(b)	Explain bus organization for four processor register and ALU connected through common buses.	07

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